



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

10/597,153

07/13/2006

Noriaki Saito

40601

6842

52054

7590

09/03/2009

PEARNE & GORDON LLP
1801 EAST 9TH STREET
SUITE 1200
CLEVELAND, OH 44114-3108

EXAMINER

TSE, YOUNG TOI

ART UNIT

PAPER NUMBER

2611

NOTIFICATION DATE

DELIVERY MODE

09/03/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patdocket@pearne.com
dchervenak@pearne.com

| | | | |
|------------------------------|--------------------------------------|-------------------------------------|--|
| Office Action Summary | Application No. 10/597,153 | Applicant(s) SAITO ET AL. | |
| | Examiner YOUNG T. TSE | Art Unit 2611 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 June 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10 and 11 is/are rejected.
- 7) ☒ Claim(s) 9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>20090616</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on June 16, 2009 have been fully considered but they are not persuasive.

Argument:

Applicants argue that it is acknowledged in the Office action that the examiner says the prior art date of the Hara reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C 102(e)). However, the Hara reference was filed after November 29, 2000 (filed on Aug. 10, 2004), thus it cannot be applied for the pre-AIPA 35 U.S.C. 102(e) rejection.

Moreover, as the international publication (WO 2005/036739) of the Hara reference was not published in English (it was published in Japanese) under PCT Article 21(2), its 35 U.S.C.102(e) priority date does not exist.

Regarding 35 U.S.C. 102 (a) and 102 (b) rejections, the international filing date of this application (January 11, 2005) predates the international application's (WO 2005/036739) publication date (April 21, 2005) as well. Therefore, both 35 U.S.C. 102 (a) and 102 (b) rejections cannot be applied based on the Hara reference. Also, the priority application (JP2003-348243) of the Hara reference was published after the international filing date of this application, and is not applicable either.

Thus, it is respectfully requested that the claim rejections under 35 U.S.C. 102 be withdrawn.

Art Unit: 2611

Response:

Applicant's arguments have been fully considered by the examiner. However, the PCT/JP05/00179 and the two foreign priority applications JAPAN 2004-017955 and JAPAN 2004-352464 are all published in Japanese. In other words, they were not published in English. Further, without the copies of the two foreign priority applications, it is unable to determine that are the present claims directly related to the invention of the two foreign priority applications since the filing date of Hara reference was filed on August 10, 2004, which was filed at least earlier than one of the two foreign priority applications.

Therefore, the rejection of claims 1-3, 7-8 and 11 under 35 U.S.C. 102(e) and the rejection of claims 4 and 6 under 35 U.S.C 103(a) are being unpatentable over the prior art.

Claim Objections

2. Claims 3 and 6-9 are objected to because of the following informalities:

Claim 3, line 7, the term "the transmission output control signal" is more accurate to read "the output control input terminal".

Claims 6-8 are objected to because they each depends from claim 3.

Claim 9, line 5, "the power supply voltage" should be "power supply voltage".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-3, 7-8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Hara et al. (US 2006/0046666, hereinafter “Hara”).

Hara discloses different transmitter embodiments, for example, shown in Figures 1 and 8, where linear operating mode or saturation operation mod set as the operation mode of a high-frequency power amplifier (15) on the basis of an operating mode set signal (107). A gain of a variable gain amplifier (14) is provided in front of the high-frequency power gain amplifier (15) and values of output voltage (109) and bias current supplied from a supply voltage/bias current control circuit (17) to the high-frequency power amplifier (15) are switched. The gain of the variable gain amplifier (14) in the saturation operation mode is formed so as to be higher by a predetermined value than

Art Unit: 2611

that in the high-frequency power amplifier (15) operates in the designated operation mode, so that the output transmission power range can be widened (abstract). Also see paragraphs [0012], [0013], [0016] - [0019], [0021] – [0031], [0033], [0036], [0038], [0039], [0052], [0055], [0059], [0062], [0063], [0070], [0074] - [0080], [0082] – [0091], and [0093] – [0095].

Regarding claim 1, the transmitter shown in either Figure 1 or Figure 8 comprising: a quadrature phase modulation unit (12 or 32) which inputs an in-phase component and a quadrature component of an input modulation signal (101) and performs quadrature modulation; a variable gain amplifier (13 or 14) which amplifies an output of the quadrature phase modulation unit with a gain being controlled based on a gain control signal (106, 107, 108); and a high-frequency power amplifier (15) which performs power amplification of an output of the variable gain amplifier. Wherein the high-frequency power amplifier has a linear mode for performing power amplification using a linear operation region in an input/output power characteristic (see Figure 5) and a saturation mode for performing power amplification using a saturation operation region in the input/output power characteristic, and wherein, if transmission output power of the high-frequency power amplifier is equal to or greater than a predetermined value, the output level of the variable gain amplifier is adjusted, the high-frequency power amplifier is operated in the saturation mode, and a transmission output control signal amplitude-modulated based on an amplitude component of the input modulation signal is input to an output control input terminal of the high-frequency power amplifier for performing polar coordinate modulation; if the transmission output power is less than

Art Unit: 2611

the predetermined value, the output level of the variable gain amplifier is adjusted, the power is operated in the linear mode, and a transmission output control signal of a predetermined level responsive to the transmission output power is input to the output control input terminal for performing linear amplification.

Regarding claim 2, wherein, if the transmission output power is at a maximum output level or in proximity thereof, the high-frequency power amplifier performs the polar coordinate modulation and if the transmission output power is smaller than the maximum output level or the proximity thereof, the power unit performs the linear amplification. Also see paragraphs [0082] and [0087].

Regarding claim 3, wherein the high-frequency power amplifier comprises a power supply terminal (109) used as the output control input terminal, and wherein the transmitter further comprises a power supply driver (17) for increasing the current capacity of the signal of the predetermined level or the signal amplitude-modulated based on the amplitude component of the input modulation signal and supplying power to the power supply terminal as the transmission output control signal.

Regarding claim 7, inherently, the supply voltage/bias current control circuit (17) comprises a liner regulator because the high-frequency power amplifier (15) is operated in either linear operation mode or saturation operation mode.

Regarding claim 8, inherently, the supply voltage/bias current control circuit (17) comprises a switching regulator in order to control the voltage and/or bias current to the high-frequency power amplifier (15).

Regarding claim 11, Hara teaches that the transmitter used in either Figure 1 or Figure 8 can be applied to a radio communication apparatus such as a portable wireless terminal apparatus or a radio base station (paragraph [0110]).

5. Claims 1-8 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al. (US 2005/0135502, hereinafter "Zhang").

Zhang discloses an RF transmitter 380 in Figure 3, which provides both GSM and EDGE capability by implementing collector voltage control over the power transistors in a power amplifier 330. During EDGE mode, linear base-biasing a power amplifier (PA) allows collector control to provide either saturated mode PA operation (during ramp up/ramp down) or linear mode PA operation (during data burst). Collector control can therefore be used to provide the accurate ramp up and ramp down profiles required for both GSM and EDGE burst output signals, and can also be used to set the level of the constant envelope data operation can provide the non-constant envelope EDGE data burst. A variable gain amplifier 320 is used to adjust the input signal to the power amplifier such that the desired transmission level is achieved. See abstract and the detailed description of Figure 3 from paragraph [0043] to paragraph [0071].

Figure 6 shows the detailed block elements of the power amplifier 330 and the collector control circuit 340 which also includes the base bias circuit 350 of Figure 3. The detailed description of Figure 6 is described from paragraph [0077] to paragraph [0093].

Regarding claim 1, the RF transmitter shown in Figure 3 comprises an upconverter circuit 310 including a quadrature phase or amplitude modulation circuit

Art Unit: 2611

311 (paragraph [0046]), which inputs an in-phase component and a quadrature component of an input modulation signal S(D3) and performs quadrature modulation; a variable gain amplifier (VGA) 320 which amplifies an output of the upconverter circuit 310 with a gain being controlled based on a gain control signal S(VGA); and a high-frequency power amplifier 330 which performs power amplification of an output of the variable gain amplifier.

Wherein the high-frequency power amplifier has a linear mode for performing power amplification using a linear operation region in an input/output power characteristic S(B3) and a saturation mode for performing power amplification using a saturation operation region in the input/output power characteristic, and wherein, if transmission output power of the high-frequency power amplifier is equal to or greater than a predetermined value, the output level of the variable gain amplifier is adjusted, the high-frequency power amplifier is operated in the saturation mode, and a transmission output control signal amplitude-modulated based on an amplitude component of the input modulation signal is input to an output control input terminal of the high-frequency power amplifier for performing polar coordinate modulation; if the transmission output power is less than the predetermined value, the output level of the variable gain amplifier is adjusted, the power is operated in the linear mode, and a transmission output control signal of a predetermined level responsive to the transmission output power is input to the output control input terminal for performing linear amplification. Paragraphs [0054], [0060], [0069], [0083], [0084], [0086], and [0089].

Regarding claim 2, wherein, if the transmission output power is at a maximum output level or in proximity thereof, the high-frequency power amplifier performs the polar coordinate modulation and if the transmission output power is smaller than the maximum output level or the proximity thereof, the power unit performs the linear amplification. Paragraphs [0069], [0084], and [0085].

Regarding claims 3 and 6, for example, in Figure 6, the collector control circuit 340 corresponds to the power supply driver comprising an operational amplifier 343 for increasing the current capacity of the signal of the predetermined level or the signal amplitude-modulated based on the amplitude component of the input modulation signal and supplying power to the power supply terminal S(B3) as the transmission output control signal.

Regarding claim 4, a fixed voltage VBATT is provided to the collector control circuit 340 and a base bias circuit 350 is coupled between the collector control circuit 340 and the power amplifier 330.

Regarding claim 5, although Zhang fails to mention the switching operation of changing an operation clock by the DAC converter 301A and/or 301B between the linear amplification and the polar coordinate or amplitude or phase modulation of the power amplifier 330. It is inherent and/or well known to a skilled person in the art that a DAC converter is being controlled by a clock control circuit to determine the speed or the transmission rate of the incoming received signal. Inherently, since the speed of transmission rate of the linear amplification is much slower than the polar coordinate or amplitude or phase modulation of the power amplifier 330, therefore, the linear

Art Unit: 2611

amplification must be operated with a higher operation clock than the polar coordinate or amplitude or phase modulation in the power amplifier 330 in order to synchronize the operation between the linear communication mode and the saturated communication mode.

Regarding claims 7 and 8, since the power amplifier 330 can be switched between the saturated mode and the linear mode, the collector control circuit 340 is capable of operating in a liner regulator and/or a switching regulator. Paragraph [0089].

Regarding claim 11, Zhang teaches that the RF transmitter is capable of implemented in wireless communications technologies. Paragraph [0002].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

Art Unit: 2611

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hara.

As described in paragraph 8 above, although Hara does not explicitly show, teach, or suggest that a power supply terminal provided by the supply voltage/bias current control circuit (17) provides a fixed power supply as the control signal to control the high-frequency power amplifier (15). It is obvious to an average skilled artisan would recognize that any power supply device, such as the supply voltage/bias current control circuit (17) is capable of supplying either a variable voltage or a fixed voltage to provide a control voltage to a power amplifier, such as the high-frequency power amplifier (15).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hara in view of Mattila et al (US 5,432,473, hereinafter "Mattila").

Regarding claim 6, although Hara does not show the detailed block diagram of the supply voltage/bias current control circuit (17) that comprises an operational amplifier for waveform shaping, and wherein the operational amplifier can change an operation current and has an operation current switch function for increasing the operation current as compared with that when the linear amplification is performed only when polar coordinate modulation is performed in the high-frequency power amplifier.

Mattila discloses a transmitter in Figure 1 comprising similar block element to Hara's transmitter, such as variable gain amplifier (1, 2), power amplifier (3), and bias

Art Unit: 2611

control circuit (7) for controlling the voltages of the driver amplifier (2) and the power amplifier (3).

Figure 2 shows the detailed block diagram of the bias control circuit (7) of Figure 1 which clearly comprises an operational amplifier (N21) changes an operation current and has an operation current switch function for increasing the operation current as compared with the performance of the power amplifier (3). See col. 4, lines 23-66.

Therefore, it would have been obvious to one of ordinary skill in the art that a voltage/bias current control circuit, such as Hara's supply voltage/bias current control circuit (17), comprising an operational amplifier as taught by Mattila which is capable of changing an operation current and has an operation current switch function for increasing the operation current as compared with that when the linear amplification is performed only when polar coordinate modulation is performed in the high-frequency power amplifier (15).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hara in view of Bengtsson et al. (US 2002/0071497, hereinafter "Bengtsson").

Regarding claim 10, although Hara does not show a feedback section of a receiver circuit comprising a demodulation section for demodulating an output of the high-frequency power amplifier (15) and a control section for adjusting the timing of amplitude modulation when polar coordinate modulation is performed in the high-frequency power amplifier based on information of a demodulation signal provided by the demodulation section.

Bengtsson discloses a transmitter circuit in different embodiments, such as the one shown in Figure 6, which comprises similar block elements, such as the quadrature modulation circuit (420), a gain control circuit (430') and the power amplifier (460). Figure 6 also comprises a feedback receiver circuit (440') including a demodulation circuit (533) for demodulating the output signal of the power amplifier (46)) and a control circuit (446, 442, 443) for controlling the gain of the power amplifier (460). Also see paragraphs [0032] and [0033].

Therefore, it would have been obvious to one of ordinary skill in the art as taught by Bengtsson to employ a feedback receiver circuit including a demodulation circuit and a control circuit in Hara's transmitter in order to control the gain of the high-frequency power amplifier (15) and to adjust the timing of amplitude modulation when polar coordinate modulation is performed in the high-frequency power amplifier based on information of a demodulation signal provided by the demodulation circuit.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al in view of Hadjichristos (US 2004/0219891).

Regarding claim 10, although Zhang does not show a feedback section of a receiver circuit comprising a demodulation section for demodulating an output of the power amplifier 330 and a control section for adjusting the timing of amplitude modulation when polar coordinate modulation is performed in the power amplifier based on information of a demodulation signal provided by the demodulation section.

Hadjichristos discloses a polar modulation transmitter circuit 30, for example, shown in Figure 5, which comprises a demodulation circuit 92 within an ACPR

Art Unit: 2611

measurement circuit 82, which corresponds to the output signal of the power amplifier 36 and a control circuit 84 for controlling the timing of the amplitude and/or phase of the modulator 34. Paragraphs [0059] and [0060].

Therefore, it would have been obvious to one of ordinary skill in the art as taught by Hadjichristos to employ a feedback receiver circuit including a demodulation circuit and a control circuit in Zhang's RF transmitter in order to control the gain of the power amplifier 330 and to adjust the timing of amplitude modulation of the modulator 310 when polar coordinate modulation is performed in the power amplifier based on information of a demodulation signal provided by the demodulation circuit.

Allowable Subject Matter

12. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sanders relates to power amplifier mode control and an associated switching arrangement permit a wireless communications device, such as a mobile terminal, to advantageously use the same transmitter power amplifier in both digital and analog operating modes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to YOUNG T. TSE whose telephone number is 571- 272-3051. The examiner can normally be reached on Monday-Friday 10:00-6:30 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on 571- 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/YOUNG T. TSE/
Primary Examiner, Art Unit 2611